# Chapter 5:
# Field–Effect Transistors

**Robert Boylestad**
*Digital Electronics*


**Slide 1**

## FET

FET's (Field – Effect Transistors) are much like BJT's (Bipolar Junction Transistors).

**Similarities:**

- Amplifiers
- Switching devices
- Impedance matching circuits

**Differences:**

- FET's are voltage controlled devices whereas BJT's are current controlled devices.
- FET's also have a higher input impedance, but BJT's have higher gains.
- FET's are less sensitive to temperature variations and because of there construction they are more easily integrated on IC's.
- FET's are also generally more static sensitive than BJT's.

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*Digital Electronics*
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## FET Types

- **JFET** ~ Junction Field-Effect Transistor
- **MOSFET** ~ Metal-Oxide Field-Effect Transistor
  - **D-MOSFET** ~ Depletion MOSFET
  - **E-MOSFET** ~ Enhancement MOSFET




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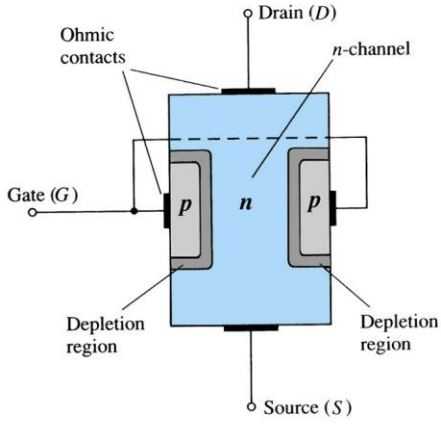
## JFET Construction

There are two types of JFET's: n-channel and p-channel.
The n-channel is more widely used.




There are three terminals: Drain (D) and Source (S) are connected to n-channel
Gate (G) is connected to the p-type material

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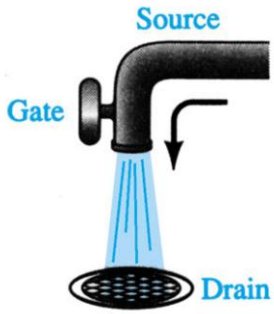
## Basic Operation of JFET

JFET operation can be compared to a water spigot:




The source of water pressure – accumulated electrons at the negative pole of the applied voltage from Drain to Source

The drain of water – electron deficiency (or holes) at the positive pole of the applied voltage from Drain to Source.

The control of flow of water – Gate voltage that controls the width of the n-channel, which in turn controls the flow of electrons in the n-channel from source to drain.

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## JFET Operating Characteristics

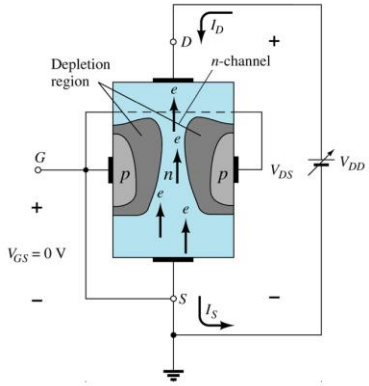
There are three basic operating conditions for a JFET:

A. $V_{GS} = 0$, $V_{DS}$ increasing to some positive value

B. $V_{GS} < 0$, $V_{DS}$ at some positive value

C. Voltage-Controlled Resistor

**Slide 6** **A. $V_{GS} = 0$, $V_{DS}$ increasing to some positive value**

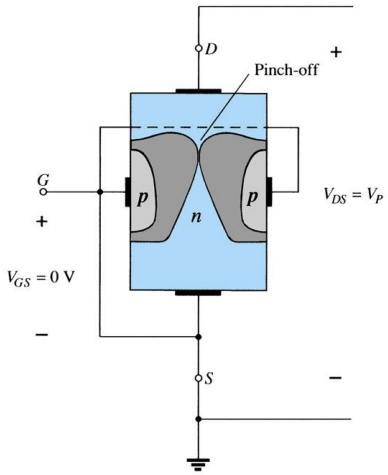



Three things happen when $V_{GS} = 0$ and $V_{DS}$ is increased from 0 to a more positive voltage:

- the depletion region between p-gate and n-channel increases as electrons from n-channel combine with holes from p-gate.
- increasing the depletion region, decreases the size of the n-channel which increases the resistance of the n-channel.
- But even though the n-channel resistance is increasing, the current ($I_D$) from Source to Drain through the n-channel is increasing. This is because $V_{DS}$ is increasing.




**Slide 7** **Pinch-off**




If $V_{GS} = 0$ and $V_{DS}$ is further increased to a more positive voltage, then the depletion zone gets so large that it ***pinches off*** the n-channel. This suggests that the current in the n-channel ($I_D$) would drop to 0A, but it does just the opposite: as $V_{DS}$ increases, so does $I_D$.

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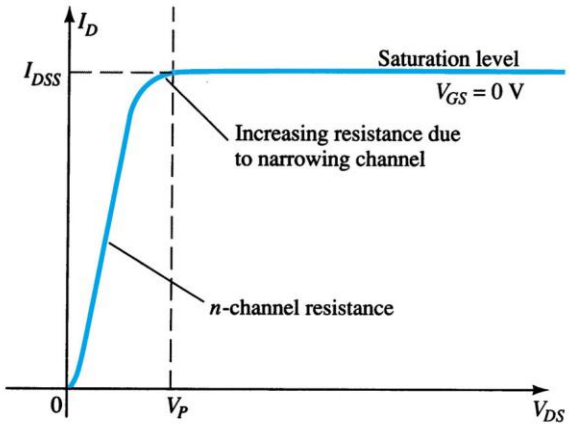
## Saturation




At the pinch-off point:

- any further increase in $V_{GS}$ does not produce any increase in $I_D$. $V_{GS}$ at pinch-off is denoted as Vp.
- ID is at saturation or maximum. It is referred to as $I_{DSS}$.
- The ohmic value of the channel is at maximum.

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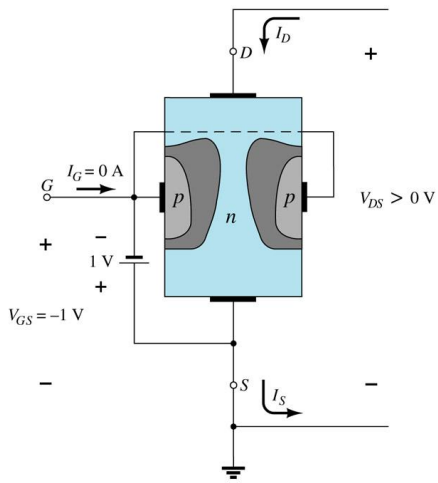
## B. $V_{GS} < 0$, $V_{DS}$ at some positive value




As $V_{GS}$ becomes more negative the depletion region increases.

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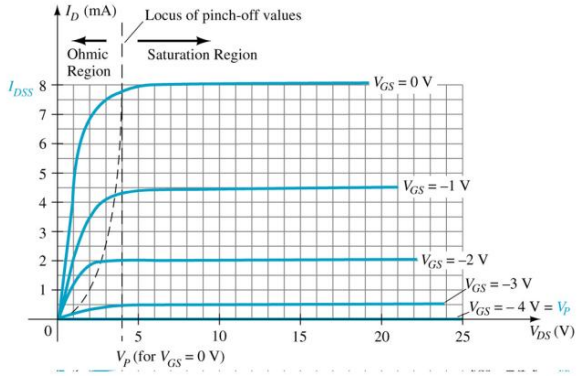
## $I_D < I_{DSS}$




As $V_{GS}$ becomes more negative:

- the JFET will pinch-off at a lower voltage (Vp).
- $I_D$ decreases ($I_D < I_{DSS}$) even though $V_{DS}$ is increased.
- Eventually $I_D$ will reach 0A. $V_{GS}$ at this point is called Vp or $V_{GS(off)}$.
- Also note that at high levels of $V_{DS}$ the JFET reaches a breakdown situation. ID will increases uncontrollably if $V_{DS} > V_{DSmax}$.

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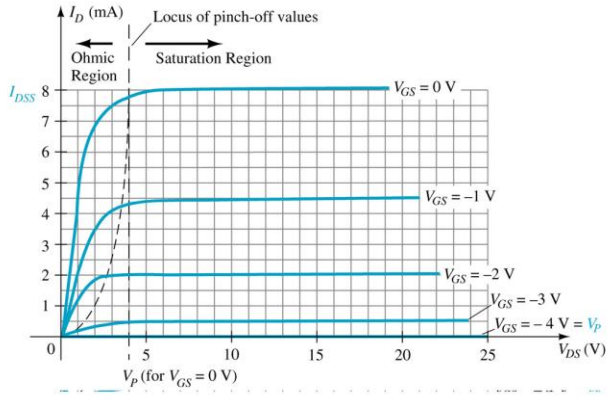
## C. Voltage-Controlled Resistor




The region to the left of the pinch-off point is called the ***ohmic region***.
The JFET can be used as a variable resistor, where VGS controls the drain-source resistance (rd). As $V_{GS}$ becomes more negative, the resistance (rd) increases.

$$r_d = \frac{r_o}{\left(1 - \frac{V_{GS}}{V_P}\right)^2} \qquad \text{[Formula 5.1]}$$

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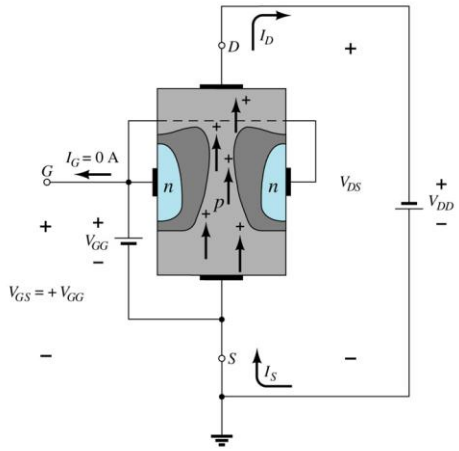
## p-Channel JFETS




p-Channel JFET acts the same as the n-channel JFET, except the polarities and currents are reversed.

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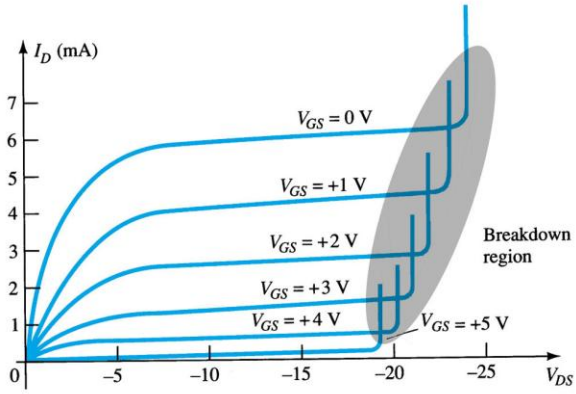
## P-Channel JFET Characteristics




As VGS increases more positively:

- the depletion zone increases
- $I_D$ decreases ($I_D < I_{DSS}$)
- eventually $I_D = 0$A

Also note that at high levels of VDS the JFET reaches a breakdown situation. ID increases uncontrollably if $V_{DS} > V_{DSmax}$.

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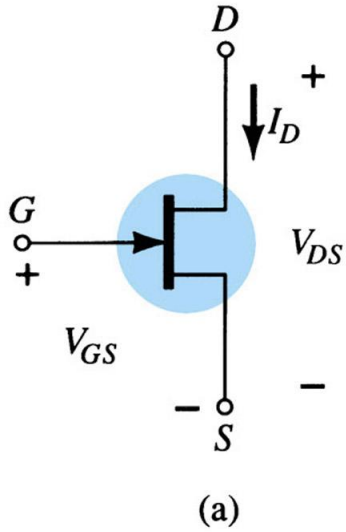
## JFET Symbols







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## Transfer Characteristics

The transfer characteristic of input-to-output is not as straight forward in a JFET as it was in a BJT.

In a BJT, β indicated the relationship between $I_B$ (input) and $I_C$ (output).

In a JFET, the relationship of $V_{GS}$ (input) and $I_D$ (output) is a little more complicated:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \qquad \text{[Formula 5.3]}$$

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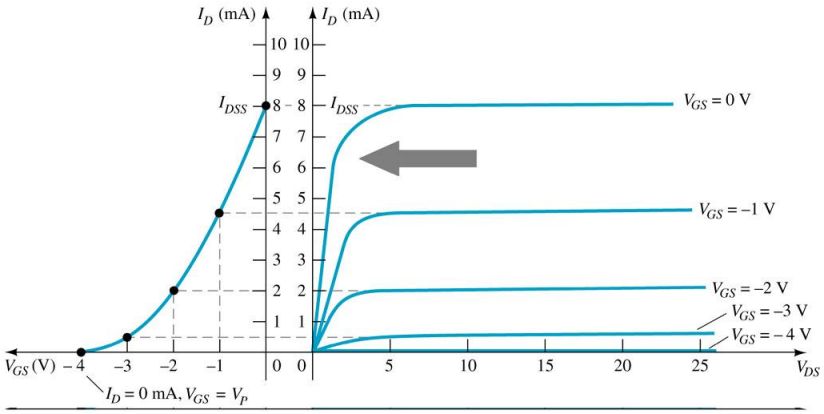
## Transfer Curve




From this graph it is easy to determine the value of $I_D$ for a given value of $V_{GS}$.

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## Plotting the Transfer Curve

Using $I_{DSS}$ and Vp ($V_{GS(off)}$) values found in a specification sheet, the Transfer Curve can be plotted using these 3 steps:

Step 1: $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$ [Formula 5.3]

Solving for $V_{GS} = 0V$: $I_D = I_{DSS}$ at $V_{GS} = 0V$ [Formula 5.4]

Step 2: $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$ [Formula 5.3]

Solving for $V_{GS}$ = Vp ($V_{GS(off)}$): $I_D = 0A$ at $V_{GS} = V_P$ [Formula 5.5]

Step 3:

Solving for $V_{GS}$ = 0V to Vp: $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$ [Formula 5.3]

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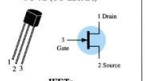
## Specification Sheet (JFETs)

**2N5457**
CASE 29-04, STYLE 5
TO-92 (TO-226AA)




**JFETs**
**GENERAL PURPOSE**
**N-CHANNEL—DEPLETION**

Refer to 2N4220 for graphs.

**MAXIMUM RATINGS**

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain-Source Voltage | $V_{DS}$ | 25 | Vdc |
| Drain-Gate Voltage | $V_{DG}$ | 25 | Vdc |
| Reverse Gate-Source Voltage | $V_{GSR}$ | –25 | Vdc |
| Gate Current | $I_G$ | 10 | mAdc |
| Total Device Dissipation @ $T_A$ = 25°C<br>Derate above 25°C | $P_D$ | 310<br>2.82 | mW<br>mW/°C |
| Junction Temperature Range | $T_J$ | 125 | °C |
| Storage Channel Temperature Range | $T_{stg}$ | –65 to +150 | °C |

**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Gate-Source Breakdown Voltage ($I_G$ = –10 μAdc, $V_{DS}$ = 0) | | $V_{(BR)GSS}$ | –25 | – | – | Vdc |
| Gate Reverse Current ($V_{GS}$ = –15 Vdc, $V_{DS}$ = 0)<br>($V_{GS}$ = –15 Vdc, $V_{DS}$ = 0, $T_A$ = 100°C) | | $I_{GSS}$ | –<br>– | –<br>– | –1.0<br>–200 | nAdc |
| Gate Source Cutoff Voltage ($V_{DS}$ = 15 Vdc, $I_D$ = 10 nAdc) | 2N5457 | $V_{GS(off)}$ | –0.5 | – | –6.0 | Vdc |
| Gate Source Voltage ($V_{DS}$ = 15 Vdc, $I_D$ = 100 μAdc) | 2N5457 | $V_{GS}$ | – | –2.5 | – | Vdc |
| **ON CHARACTERISTICS** | | | | | | |
| Zero-Gate-Voltage Drain Current* ($V_{DS}$ = 15 Vdc, $V_{GS}$ = 0) | 2N5457 | $I_{DSS}$ | 1.0 | 3.0 | 5.0 | mAdc |
| **SMALL-SIGNAL CHARACTERISTICS** | | | | | | |
| Forward Transfer Admittance Common Source* ($V_{DS}$ = 15 Vdc, $V_{GS}$ = 0, f = 1.0 kHz) | 2N5457 | $\|y_{fs}\|$ | 1000 | – | 5000 | μmhos |
| Output Admittance Common Source* ($V_{DS}$ = 15 Vdc, $V_{GS}$ = 0, f = 1.0 kHz) | | $\|y_{os}\|$ | – | 10 | 50 | μmhos |
| Input Capacitance ($V_{DS}$ = 15 Vdc, $V_{GS}$ = 0, f = 1.0 MHz) | | $C_{iss}$ | – | 4.5 | 7.0 | pF |
| Reverse Transfer Capacitance ($V_{DS}$ = 15 Vdc, $V_{GS}$ = 0, f = 1.0 MHz) | | $C_{rss}$ | – | 1.5 | 3.0 | pF |

*Pulse Test: Pulse Width ≤ 630 ms; Duty Cycle ≤ 10%.

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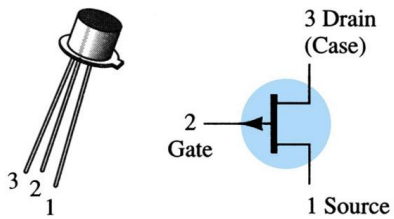
## Case Construction and Terminal Identification

**2N2844**
CASE 22-03, STYLE 12
TO-18 (TO-206AA)




**JFETs**
**GENERAL PURPOSE**
**P-CHANNEL**

This information is also available on the specification sheet.

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## Testing JFET

a. Curve Tracer – This will display the ID versus VDS graph for various levels of VGS.

b. Specialized FET Testers – These will indicate IDSS for JFETs.




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## MOSFETs

MOSFETs have characteristics similar to JFETs and additional characteristics that make then very useful.

There are 2 types:

- Depletion-Type MOSFET
- Enhancement-Type MOSFET

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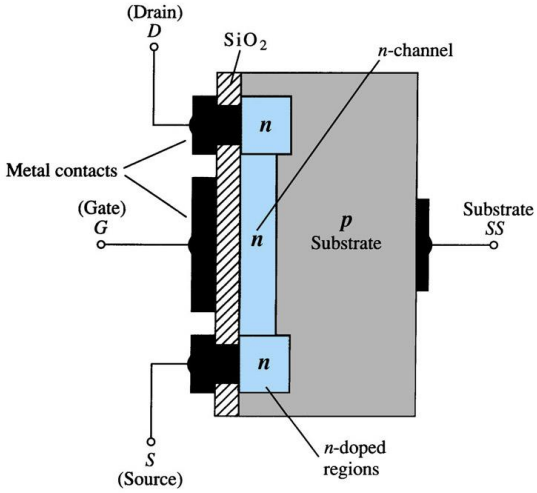
## Depletion-Type MOSFET Construction




The Drain (D) and Source (S) connect to the to n-doped regions. These N-doped regions are connected via an n-channel. This n-channel is connected to the Gate (G) via a thin insulating layer of $SiO_2$. The n-doped material lies on a p-doped substrate that may have an additional terminal connection called SS.

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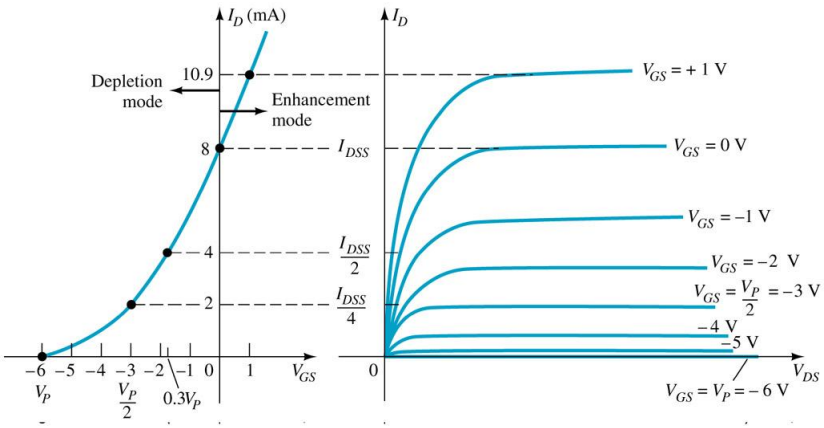
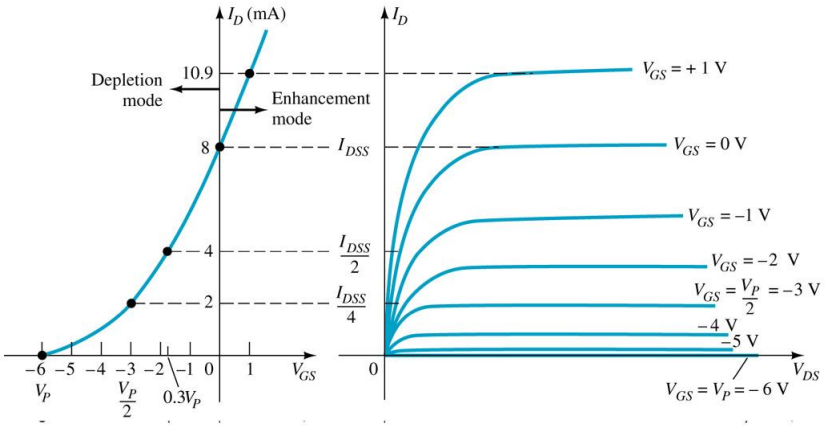
## Basic Operation

A Depletion MOSFET can operate in two modes: Depletion or Enhancement mode.



## Slide 24 Depletion-type MOSFET in Depletion Mode




**Depletion mode**

The characteristics are similar to the JFET.

When $V_{GS} = 0V$, $I_D = I_{DSS}$

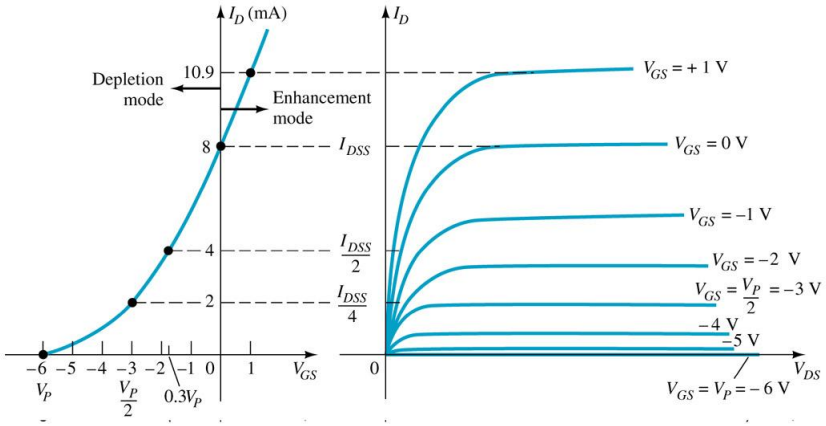
When $V_{GS} < 0V$, $I_D < I_{DSS}$

The formula used to plot the Transfer Curve still applies:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$ [Formula 5.3]




## Slide 25 Depletion-type MOSFET in Enhancement Mode




**Enhancement mode**

$V_{GS} > 0V$, $I_D$ increases above $I_{DSS}$

The formula used to plot the Transfer Curve still applies:

(note that VGS is now a positive polarity)

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$ [Formula 5.3]

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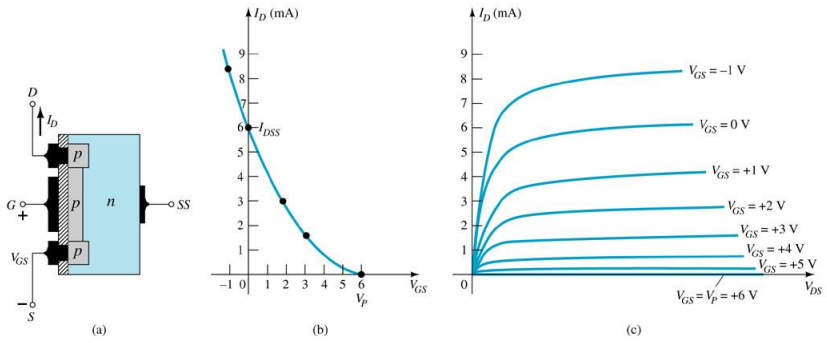
## p-Channel Depletion-Type MOSFET




The p-channel Depletion-type MOSFET is similar to the n-channel except that the voltage polarities and current directions are reversed.

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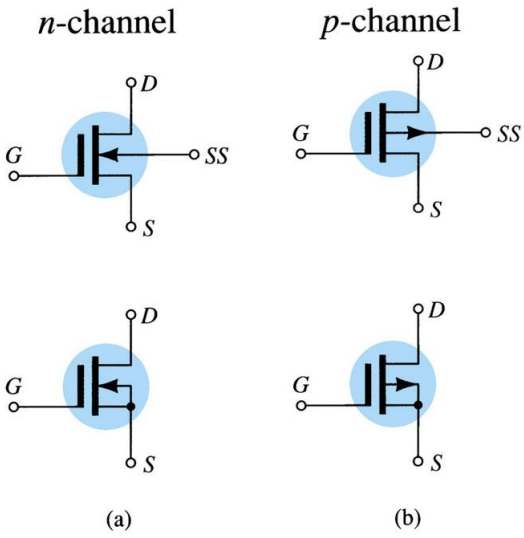
## Symbols



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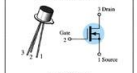
## Specification Sheet

**2N3797**

CASE 22-03, STYLE 2
TO-18 (TO-206AA)




**MOSFETs**
**LOW POWER AUDIO**
**N-CHANNEL – DEPLETION**

**MAXIMUM RATINGS**

| Rating | | Symbol | Value | Unit |
|---|---|---|---|---|
| Drain–Source Voltage | 2N3797 | $V_{DS}$ | 20 | Vdc |
| Gate–Source Voltage | | $V_{GS}$ | ±10 | Vdc |
| Drain Current | | $I_D$ | 20 | mAdc |
| Total Device Dissipation @ $T_A$ = 25°C<br>Derate above 25°C | | $P_D$ | 200<br>1.14 | mW<br>mW/°C |
| Junction Temperature Range | | $T_J$ | +175 | °C |
| Storage Channel Temperature Range | | $T_{stg}$ | -65 to +200 | °C |

**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain Source Breakdown Voltage ($V_{GS}$ = -7.0 V, $I_D$ = 5.0 μA) | 2N3797 | $V_{(BR)DSS}$ | 20 | 25 | – | Vdc |
| Gate Reverse Current (1) ($V_{GS}$ = -10 V, $V_{DS}$ = 0)<br>($V_{GS}$ = -10 V, $V_{DS}$ = 0, $T_A$ = 150°C) | | $I_{GSS}$ | –<br>– | –<br>– | 1.0<br>200 | pAdc |
| Gate Source Cutoff Voltage ($I_D$ = 2.0 μA, $V_{DS}$ = 10 V) | 2N3797 | $V_{GS(off)}$ | – | -5.0 | -7.0 | Vdc |
| Drain-Gate Reverse Current (1) ($V_{DG}$ = 10 V, $I_S$ = 0) | | $I_{DGO}$ | – | – | 1.0 | pAdc |
| **ON CHARACTERISTICS** | | | | | | |
| Zero-Gate-Voltage Drain Current ($V_{DS}$ = 10 V, $V_{GS}$ = 0) | 2N3797 | $I_{DSS}$ | 2.0 | 2.9 | 6.0 | mAdc |
| On-State Drain Current ($V_{DS}$ = 10 V, $V_{GS}$ = +3.5 V) | 2N3797 | $I_{D(on)}$ | 9.0 | 14 | 18 | mAdc |
| **SMALL-SIGNAL CHARACTERISTICS** | | | | | | |
| Forward Transfer Admittance ($V_{DS}$ = 10 V, $V_{GS}$ = 0, f = 1.0 kHz) | 2N3797 | $\|Y_{fs}\|$ | 1500 | 2300 | 3000 | μmhos |
| ($V_{DS}$ = 10 V, $V_{GS}$ = 0, f = 1.0 MHz) | 2N3797 | | 1500 | – | – | |
| Output Admittance ($I_{DS}$ = 10 V, $V_{GS}$ = 0, f = 1.0 kHz) | 2N3797 | $\|Y_{os}\|$ | – | 27 | 60 | μmhos |
| Input Capacitance ($V_{DS}$ = 10 V, $V_{GS}$ = 0, f = 1.0 MHz) | 2N3797 | $C_{iss}$ | – | 6.0 | 8.0 | pF |
| Reverse Transfer Capacitance ($V_{DS}$ = 10 V, $V_{GS}$ = 0, f = 1.0 MHz) | | $C_{rss}$ | – | 0.5 | 0.8 | pF |
| **FUNCTIONAL CHARACTERISTICS** | | | | | | |
| Noise Figure ($V_{DS}$ = 10 V, $V_{GS}$ = 0, f = 1.0 kHz, $R_G$ = 3 megohms) | | NF | – | 3.8 | – | dB |

(1) This value of current includes both the FET leakage current as well as the leakage current associated with the test socket and fixture when measured under best attainable conditions.

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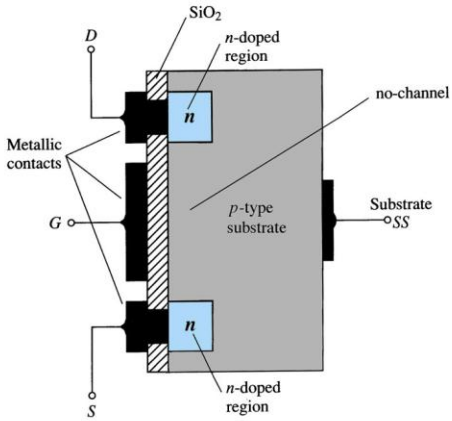
## Enhancement-Type MOSFET Construction




The Drain (D) and Source (S) connect to the to n-doped regions. These n-doped regions are connected via an n-channel. The Gate (G) connects to the p-doped substrate via a thin insulating layer of $SiO_2$. There is no channel. The n-doped material lies on a p-doped substrate that may have an additional terminal connection called SS.

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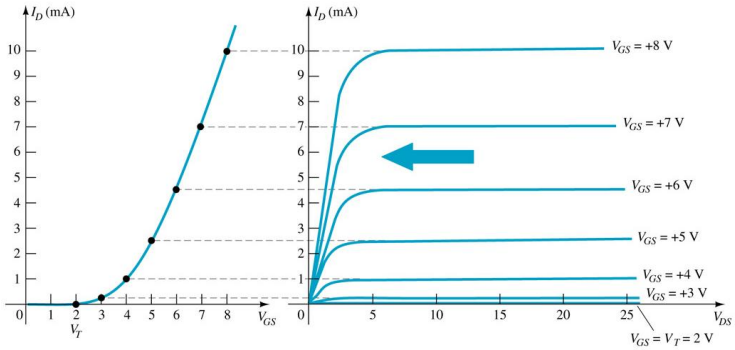
## Basic Operation

The Enhancement-type MOSFET only operates in the enhancement mode.




$V_{GS}$ is always positive
As $V_{GS}$ increases, $I_D$ increases
But if $V_{GS}$ is kept constant and $V_{DS}$ is increased, then $I_D$ saturates ($I_{DSS}$)
The saturation level, $V_{DSsat}$ is reached.

$$V_{Dsat} = V_{GS} - V_T \qquad \text{[Formula 5.12]}$$

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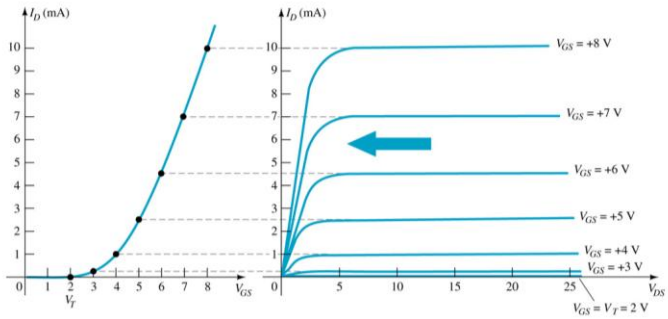
## Transfer Curve




To determine $I_D$ given $V_{GS}$: $I_D = k(V_{GS} - V_T)^2$ [Formula 5.13]
where $V_T$ = threshold voltage or voltage at which the MOSFET turns on.
k = constant found in the specification sheet
k can also be determined by using values at a specific point and the formula:

$$k = \frac{I_{D(on)}}{(V_{GS(ON)} - V_T)^2} \qquad \text{[Formula 5.14]}$$

$V_{DSsat}$ can also be calculated:

$$V_{Dsat} = V_{GS} - V_T \qquad \text{[Formula 5.12]}$$

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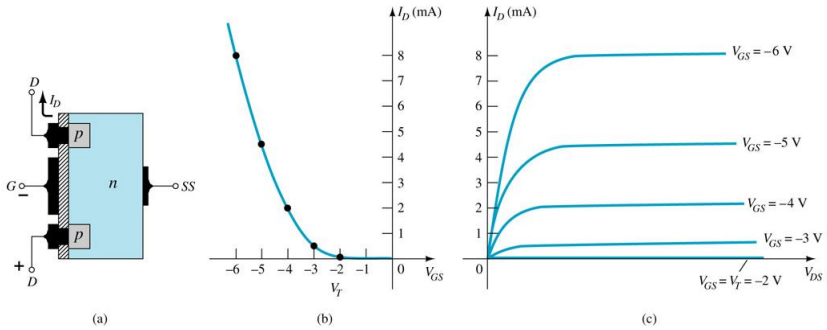
## p-Channel Enhancement-Type MOSFETs

The p-channel Enhancement-type MOSFET is similar to the n-channel except that the voltage polarities and current directions are reversed.





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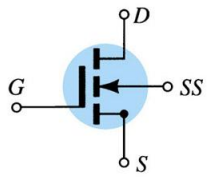
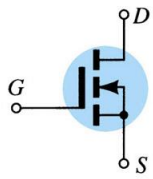
## Symbols

*n*-channel




(a)

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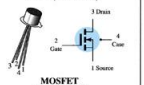
## Specification Sheet

**2N4351**
CASE 20-03, STYLE 2
TO-72 (TO-206AF)




**MOSFET**
**SWITCHING**
**N-CHANNEL – ENHANCEMENT**

**MAXIMUM RATINGS**

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–Source Voltage | $V_{DS}$ | 25 | Vdc |
| Drain–Gate Voltage | $V_{DG}$ | 30 | Vdc |
| Gate–Source Voltage* | $V_{GS}$ | 30 | Vdc |
| Drain Current | $I_D$ | 30 | mAdc |
| Total Device Dissipation @ $T_A$ = 25°C<br>Derate above 25°C | $P_D$ | 300<br>1.7 | mW<br>mW/°C |
| Junction Temperature Range | $T_J$ | 175 | °C |
| Storage Temperature Range | $T_{stg}$ | −65 to +175 | °C |

* Transient potentials of ± 75 Volt will not cause gate-oxide failure.

**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C unless otherwise noted.)

| Characteristic | | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | |
| Drain-Source Breakdown Voltage ($I_D$ = 10 μA, $V_{GS}$ = 0) | | $V_{(BR)DSX}$ | 25 | – | Vdc |
| Zero-Gate-Voltage Drain Current ($V_{DS}$ = 10 V, $V_{GS}$ = 0) | $T_A$ = 25°C<br>$T_A$ = 150°C | $I_{DSS}$ | –<br>– | 10<br>10 | nAdc<br>μAdc |
| Gate Reverse Current ($V_{GS}$ = ± 15 Vdc, $V_{DS}$ = 0) | | $I_{GSS}$ | – | ± 10 | pAdc |
| **ON CHARACTERISTICS** | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = 10 V, $I_D$ = 10 μA) | | $V_{GS(Th)}$ | 1.0 | 5 | Vdc |
| Drain-Source On-Voltage ($I_D$ = 2.0 mA, $V_{GS}$ = 10V) | | $V_{DS(on)}$ | – | 1.0 | V |
| On-State Drain Current ($V_{DS}$ = 10 V, $V_{GS}$ = 10 V) | | $I_{D(on)}$ | 3.0 | – | mAdc |
| **SMALL-SIGNAL CHARACTERISTICS** | | | | | |
| Forward Transfer Admittance ($V_{DS}$ = 10 V, $I_D$ = 2.0 mA, f = 1.0 kHz) | | $\|y_{fs}\|$ | 1000 | – | μmho |
| Input Capacitance ($V_{DS}$ = 10 V, $V_{GS}$ = 0, f = 140 kHz) | | $C_{iss}$ | – | 5.0 | pF |
| Reverse Transfer Capacitance ($V_{DS}$ = 0, $V_{GS}$ = 0, f = 140 kHz) | | $C_{rss}$ | – | 1.3 | pF |
| Drain-Substrate Capacitance ($V_{D(SUB)}$ = 10 V, f = 140 kHz) | | $C_{d(sub)}$ | – | 5.0 | pF |
| Drain-Source Resistance ($V_{GS}$ = 10 V, $I_D$ = 0, f = 1.0 kHz) | | $r_{ds(on)}$ | – | 300 | ohms |
| **SWITCHING CHARACTERISTICS** | | | | | |
| Turn-On Delay (Fig. 5) | $I_D$ = 2.0 mAdc, $V_{DS}$ = 10 Vdc,<br>($V_{GS}$ = 10 Vdc)<br>(See Figure 9; Times Circuit Determined) | $t_{d1}$ | – | 45 | ns |
| Rise Time (Fig. 6) | | $t_r$ | – | 65 | ns |
| Turn-Off Delay (Fig. 7) | | $t_{d2}$ | – | 60 | ns |
| Fall Time (Fig. 8) | | $t_f$ | – | 100 | ns |

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## MOSFET Handling

MOSFETs are very static sensitive. Because of the very thin $SiO_2$ layer between the external terminals and the layers of the device, any small electrical discharge can stablish an unwanted conduction.

**Protection:**

- Always transport in a static sensitive bag
- Always wear a static strap when handling MOSFETS
- Apply voltage limiting devices between the Gate and Source, such as back-to-back Zeners to limit any transient voltage.

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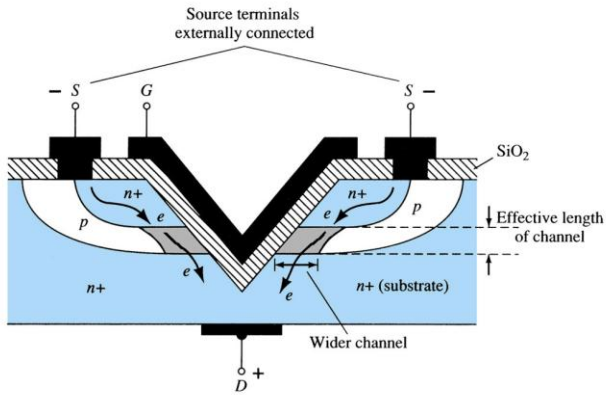
## VMOS




VMOS – Vertical MOSFET increases the surface area of the device.

**Advantage:**

- This allows the device to handle higher currents by providing it more surface area to dissipate the heat.
- VMOSs also have faster switching times.

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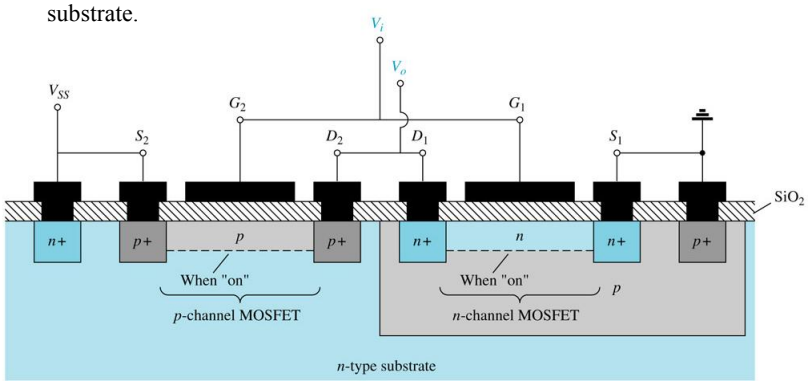
## CMOS

CMOS – Complementary MOSFET p-channel and n-channel MOSFET on the same substrate.




**Advantage:**

- Useful in logic circuit designs
- Higher input impedance
- Faster switching speeds
- Lower operating power levels

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# Summary Table